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| Port Name | Function |
| A[0:M-1]\* | Address Bus (has address of the Access location in Memory) |
| T\_A[0:M-1] | Bist Address |
| DI[0:N-1] | Data In Bus |
| T\_DI[0:N-1] | Bist Data In Bus |
| DO[0:N-1]\*\* | Data Out Bus |
| CLK | Clock |
| GWE\_N | Global Read/Write Enable (low for write) |
| T\_GWE\_N | Bist Global Read/Write Enable (low for write) |
| BWE\_N[0:N-1] / BYWE\_N[0:N-1] | Bit Write Enable (low for write)  Byte Write Enable (low for write) |
| T\_BWE\_N[0:N-1] /  T\_BYWE\_N[0:N-1] | Bist Bit Write Enable (low for write)  Bist Byte Write Enable (low for write) |
| CE\_N | RAM select (active low) |
| T\_CE\_N | Bist RAM select (active low) |
| OE\_N | Output Enable (low for output) |
| T\_OE\_N | Bist Output Enable (low for output) |
| T\_BE\_N | Bist enable(active low) |
| T\_AWT\_N | Asynchronous write through(active low) |
| T\_RWM | Read Write Margin |
| XOR\_OUT | Xor output |
| SE | Scan enable (active high) |
| SI | Scan input |
| SO | Scan output |
| \* M = log2(words) \*\*\*T\_BE\_N is the select signal for built in self-test. \*\* N = Bits per word | |